Application No.: 10/036,168 **Docket No.: JCLA6880**

REMARKS

Present Status of the Application

The Office Action rejected presently-pending claims 1-2 and 13 under 35 U.S.C. 103 (a) as being unpatentable over Polzin (US 5,644,760) in view of Robertson (US 6,529,967). In addition, claims 3, 9 and 11-12 are rejected under 35 U.S.C. 103 (a) being unpatentable over Polzin(US 5,644,760) in view of Robertson (US 6,529,967) and further in view of Kubo et al.(U S 6,671,814). More, claims 14-17 are rejected under 35 U.S.C. 102 (b) being unpatentable over Huang et al. (US 5,761,479).Meanwhile, the Examiner points out claims 4-8, and 10 are allowable if rewritten in independent form including all of limitations of the base claim and any intervening claims. Upon entry of in this final action response, claims 1-17 are pending of which claims 1, 2, 14 and 17 have been amended in response to "again the features upon which applicants relied (e.g. *measuring the resistance*) are not recited in the rejected claims" as alleged by the examiner in the "**Response to Arguments**" in this final office action. Applicants hope to traverse the Examiner's rejections by providing the following arguments. Reconsideration of those claims is respectfully requested.

Discussion for objection to claim under 35 U.S.C. 103 (a)

1. Claims 1-2 and 13 under 35 U.S.C. 103 (a) as being unpatentable over Polzin (US 5,644,760, hereinafter Polzin) in view of Robertson (US6,529,967,hereinafter Robertson).

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As to claim 1, Polzin teaches An apparatus for supporting multi-processors, wherein said apparatus is coupled to a central processing unit(CPU) socket, having a plurality of connecting pins (at least abstract, col3, lines 42-52, col. 6, lines 14-26, and col. 10, lines 52-65). Robertson teaches socket connecting different types of cards with different voltages (3.3 volt, 5.0 volt) and a method to detect those types of cards including: when the socket is inserted with a first type card (e.g. 5.0 volt card), a first pin has a first equivalent resistance, and when said socked is inserted with a second type (e.g. 3.0 volt card), a first pin has a second equivalent resistance. It would have been obvious to one of ordinary skill in the art to including detecting different type of cards and a method to detect those type of cards as taught by Robertson in the system of Polzin to allow cards having different voltages to be physically inserted into the same standard connector on the system board.

As to claim 2, Robertson further teaches when said CPU socket is inserted with said first type CPU, a second pin(101) among said connecting pins has a third equivalent resistance, and when said CPU socket is inserted with said second type CPU, said second pin has a fourth equivalent resistance, wherein the third equivalent resistance is not equal to the fourth equivalent resistance, and said distinguish device is coupled to said second pin to use ~~a~~ difference between said first, second, third and said fourth equivalent resistance to determine a type of said CPU inserted in said CPU socket, and to generate a CPU select signal (FIG.3, and col. 5, line 37-col. 6, line 27).

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In response thereto, applicants consider the aforementioned examiner's allegation is not persuasive and provide the following arguments. From the abstracts of the Polzin and Pobertson, functionalities of these two cited reference are to properly selective different type of cards. The card is used as an interface of a processor. However, the present application has no this interface, instead, directly coupling the different types of processors. Furthermore, a selecting mechanism for different type of cards in Polzin and Pobertson is based on different voltages. Instead, a selecting mechanism for different type of processors in the present application is based on "when said CPU socket is inserted with said first type CPU, a first equivalent resistance is measured through a first pin among said connecting pins, and when said CPU socket is inserted with said second type CPU, a second equivalent resistance is measured through said first pin" as claimed in the amended claim1. Therefore, the selecting mechanism in Polzin and Pobertson is distinct from that in the present application. In other words, the combination of Polzin and Pobertson still fails to teach, suggest or disclose "when said CPU socket is inserted with said first type CPU, a first equivalent resistance is measured through a first pin among said connecting pins, and when said CPU socket is inserted with said second type CPU, a second equivalent resistance is measured through said first pin" as claimed in the amended claim1. Hence, the amended claim 1 is patentable over Polzin in view of Robertson.

With respect to claim 2, from Fig.3, and col. 5, line 37-col. 6, line 27 in Robertson., there only discloses four states of logic level (i.e. "1" or "0") , which is not identical to

the first to the fourth equivalent resistance in the present application. In other words, claim 2 fails to teach, suggest or disclose "when said CPU socket is inserted with said first type CPU, a third equivalent resistance is measured through a second pin among said connecting pins , and when said CPU socket is inserted with said second type CPU, a fourth equivalent resistance is measured through said second pin " as claimed in the amended claim 2. Therefore, the amended claim 2 is patentable over Robertson.

4. Claims 3, 9 and 11-12 are rejected under 35 U.S.C. 103 (a) being unpatentable over Polzin(US 5,644,760) in view of Robertson (US 6,529,967) and further in view of Kubo et al.(U S 6,671,814).

As to claim 3, Robertson further teaches the distinguish device comprises a processor select circuit, coupled to said first and said second pins to use a difference between said first, said second, said third and said fourth equivalent resistances to generate a CPU select signal (col. 6, lines 1-27 and col. 7, lines 31-47). More, Kubo teaches suspend status input signal and delay said suspend status input signal with a predetermined stop determination time (after the lapse of a predetermined time), so that said processor select circuit cuts off a connection between said first pin (disconnects the power supply line) and said processor select circuit (col. 5, lines 5-42). It would have been obvious to one of ordinary skill to include receiving suspend status input signal and delay suspend status input signal with a predetermined stop

time, so that a selective circuit cuts off the connection at pins taught by Kubo in the system of Polzin and Robertson.

As to claim 9, Robertson teaches the distinguish device comprises a processor select circuit (110), coupled to said first pin to use a difference between said first equivalent resistance and said second equivalent resistance to generate said CPU select signal (col. 6, lines 1-27, and col. 7, lines 31-47). Furthermore, Kubo teaches suspend status input signal and delay said suspend status input signal with a predetermined stop determination time (after the lapse of a predetermined time), so that said processor select circuit cuts off a connection between said first pin (disconnects the power supply line) and said processor select circuit (col. 5, lines 5-42). It would have been obvious to one of ordinary skill to include receiving suspend status input signal and delay suspend status input signal with a predetermined stop time, so that a selective circuit cuts off the connection at pins taught by Kubo in the system of Polzin and Robertson.

As to claim 11, Robertson teaches coupled to a power regulator that provides a correct source voltage to said CPU inserted in said CPU socket according to said suspend status output signal (e.g. signal from gate 112) and said CPU select signal (e.g. signal from gate 116)(col. 7, lines 7-11).

As to claim 12 , Kubo teaches activate determination control circuit that enable said processor select circuit to operate after receiving said suspend status input signal, so

as to determine said type of said CPU inserted in said CPU socket (col. 4, line 61 to col. 5 line42).

In response thereto, applicants consider the aforementioned examiner's allegation is not persuasive and provide the following arguments. From Fig. 1 and 2 and col.1, lines 15-16 in Kubo, a USB connector 1 has only four pins. However, from Fig.2 in Robertson and drawings in Polzin, the different type of cards 52and 56 have only key slots 53 and 57. Therefore, obviously, the USB connector 1 taught by Kubo can not receive the cards 52 and 56 taught by Robertson and Polzin because their arrangement of slots is inconsistent with that of USB connector 1. Furthermore, connector 100 in Robertson has two contacts 101 and 102 while the USB in Kubo has four pins so that the connector 100 is not compatible with the USB. As a result, Kubo can not be incorporated into Robertson and Polzin. Even if this incorporation is undue made, neither Robertson nor Kubo can achieve their intended purpose. Therefore, for one of ordinary skill in the art, there is no motive, suggestion or desirability for making such incorporation of Robertson, Polzin and Kubo. That is, the examiner's allegation that Kubo can be incorporated into Polzin and Kubo has no ground, which in turn can not render claim 3, 9 and 11-12 obvious. Hence, claim 3, 9 and 11-12 are patentable over Polzin in view of Robertson and further in view of Kubo.

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Discussion for objection to claim under 35 U.S.C. 102

5. *Claims 14-17 are rejected under 35 U.S.C. 102 (b) being unpatentable over Huang et al. (US 5,761,479).*

As to claim 14, Huang teaches a method for supporting multi-processors in a single motherboard, applied to a computer system (abstract) that comprises a CPU socket and a suspend status input signal, wherein the CPU socket comprises a plurality of connecting pins (e.g. pin B14, S10, A13, C14...) of which a first pin has a first equivalent resistance when a first type CPU is inserted in said CPU socket, and has a second resistance when said CPU socket is inserted with a second type CPU(COL. 20, LINES 25-28), said method comprising:

using a difference between said first equivalent resistance and said second equivalent resistance to generate a CPU select signal COL. 22 LINES 54-63) ; and

selectively connecting a plurality of first CPU signals to said corresponding connecting pins, and a plurality of second type CPU signals to said corresponding pins according to said CPU select signal (AT LEAST Fig. 10, and col. 20 lines 7-67).

As to claim 17, Huang teaches a second pin 9e.g. A13, C14, S10) among said connecting pins has a third equivalent resistance when said first type CPU is inserted in said CPU (COL. 20 LINES 65-67, COL. 21, LINES 24-67), and has a fourth equivalent resistance when said second type CPU is inserted in said CPU, and a difference between said third equivalent resistance and said fourth equivalent

resistance is used to determined said type of said CPU inserted in said CPU socket (COL. 22, LINES 1-44).

In response thereto, applicants consider the aforementioned examiner's allegation is not persuasive and provide the following arguments. From col. 20, lines 25-28 in Huang, there discloses that a circuit for identifying the model of a processor plugged in a socket is based on whether pin B14 is connected when plugged by 80486DX or 80487SX. That is, Huang does not describe that the two processors produce different resistances when they are connected to the same pins in a socket on the motherboard, as disclosed in the present application. Besides, Huang also does not describe the use of the difference in resistances produced by the two processors in order to distinguish between them, as disclosed in the present application. Therefore, a processor-selecting mechanism in Huang is distinct from that in the present application. That is, Huang fails to teach, suggest or disclose the processor-selecting mechanism based on" when said CPU socket is inserted with said first type CPU, a first equivalent resistance is measured through a first pin among said connecting pins, and when said CPU socket is inserted with said second type CPU, a second equivalent resistance is measured through said first pin" as claimed in the amended claim14. Hence, claim 14 is patentable over Huang.

With respect to dependent claims 15 and 16, they are patentable over Huang as a matter of law, for at least the following reason they contain all features of their base claim 14.

With respect to dependent claims 17, from col. 20, lines 65-57 and col. 21 lines 24-67 in Huang, there discloses different processors produce different logic level, not an equivalent resistance as claimed in the amended claim 17. Therefore, Huang fails to teach, suggest or

disclose "a third equivalent resistance is measured through a second pin among said connecting pins when said first type CPU is inserted in said CPU, and a fourth equivalent resistance is measured through said second pin when said second type CPU is inserted in said CPU" as claimed in the amended claim 17. Hence, claim 17 is patentable over Huang.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-17 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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